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PATENT

Case Docket No. VALER12.001APC
Date: February 6, 2002



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Taran, et al.
Appl. No. : 09/830,634
Filed : April 27, 2001
For : MULTILAYERED
CONNECTION PLATE
Examiner : Unknown
Group Art Unit : 2841

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(Date)

John M. Carson, Reg. No. 34,303

UNITED STATES PATENT AND TRADEMARK OFFICE

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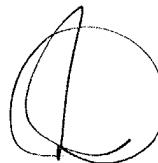
ARLINGTON, VIRGINIA 22202

ATTENTION: APPLICATION BRANCH

Dear Sir:

Enclosed for filing in the above-identified application are:

- (X) An Information Disclosure Statement.
- (X) A PTO Form 1449 with three (3) references.
- (X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.
- (X) Return prepaid postcard.



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Attorney of Record



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)

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed is form PTO-1449 listing references that are also enclosed. This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Form PTO-1449 lists foreign patent documents and other documents that are not in English. SU Patent Number 970737 discloses a multilayered printed circuit plate with a high density connection, comprising pairs of connection layers produced by means of a technological substrate and separated with electrical insulating adhesion gaskets to stick the connection layers together. The conductors of adjacent connection layers are interconnected electrically by contact nodes made in the form of a metallized through hole.

SU Patent Number 1443781 discloses a multilayered plate based on alumina ceramics. The plate has alternating ceramic layers having surfaces on which conductors are formed by applying and burning a conductive paste. The conductors of adjacent layers are coupled to each other by means of holes in the ceramic layers that are filled with a conductive paste which forms,

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after heat treating, contact nodes for connecting the conductors placed on the surfaces of adjacent layers according to a specific connection scheme.

The article entitled "The Peculiarities of Assembling the Specialized LSIC on Basic Matrix Chips" discloses a multilayered connection plate on polyimide base comprising layers of polyimide film having conductive paths placed on both surfaces of every layer. In order to couple conductors, metallized through holes of 0.1 mm in diameter are formed within every layer. To connect the layers electrically and mechanically into a multilayered printed circuit plate with the single conductor spreading topology specifically formed metallized through holes are used that are about 1.5 mm in diameter and are arranged in a matrix with a regular pitch common for all layers. The layers form after aligning the matrix of channels piercing the multilayered plate throughout. The conductors and metallized holes are formed by methods of lithography and spraying the metallization with a subsequent galvanic build-up to a required thickness and tinning those places in which should be soldered joints. Assembling the layers into a multilayered structure is performed by soldering the joints between the metallized through holes with the methods of vacuum soldering.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

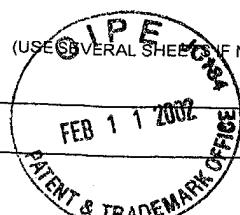
Dated: 2/6/02

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| FORM PTQ-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTY. DOCKET NO. VALER12.001APC | APPLICATION NO. 09/830,634 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | APPLICANT Taran, et al. | |
| (USE SEVERAL SHEETS IF NECESSARY) | | FILING DATE April 27, 2001 | GROUP 2841 |



U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.) |
|---------------------|--|
| | "The Peculiarities of Assembling the Specialized LSIC on Basic Matrix Chips", Moscow. "Vysshaya Shkola", 1990, pp. 31-34 |
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| EXAMINER | DATE CONSIDERED |
| <p>*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.</p> | |